REMARKS

As amended, claim 15 calls for a planarized dielectric layer filling said trench, the dielectric layer having a plurality of ions implanted into the dielectric layer.

The reference to Kamath does not teach an uncovered upper surface of the semiconductor substrate such that a dielectric, filling a trench in the substrate, and the upper surface of the semiconductor substrate are planarized. For example, as shown in Figure 6, it is evident that the upper surface of the material 142 is not planarized with the upper surface of the substrate. To the contrary, an HF etching process is utilized to remove the barrier layer 102. In contrast, if a chemical mechanical planarization step had been utilized, and the implantation conditions were appropriate, a planarized upper surface would have been achieved.

It is respectfully noted that the cited Wolf material was not included on the notice of references cited and, therefore, a copy was not provided. It is respectfully requested that the Wolf reference be made of record in the notice of references cited and that a copy be provided.

In view of these remarks, the application is now in condition for allowance.

Respectfully submitted,

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Timothy N. Trop, Reg. No. 28,994
TROP, PRUNER & HU, P.C.
8554 Katy Freeway, Ste. 100
Houston, TX 77024
713/468-8880 [Phone]
713/468-8883 [Fax]